AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for forming a contact comprising:

forming an active region;

forming a gated device having a gate in a gate region, a junction region, and a dielectric layer over the gate, the gate region and the junction region within the active region, the dielectric having a first thickness over the gate and a different second thickness over the junction region; and

forming a contact opening through the dielectric layer to the gate comprising etching for a period of time between a time necessary to etch through the dielectric layer on the gate region and a time necessary to etch through the dielectric layer and to the junction region;

forming a contact in the contact opening to ~~a~~ the gate ~~of the gated device in the active region~~.

2. (Currently Amended) The method of claim 1, wherein prior to forming the contact to the gate, the method further comprises:

~~forming a dielectric layer on the gated device in the active region;~~

forming a contact opening through the dielectric layer to a junction region of the gated device using a first mask; and

forming a contact opening through the dielectric layer to the gate of the gated device using a different second mask.

3. (Canceled)

4. (Currently Amended) The method of claim ~~2~~1, wherein prior to forming the dielectric layer on the gated device, forming a conformal etch stop layer on the junction region and the gate of the gated device.

5. (Currently Amended) The method of claim 4, wherein the forming an opening through the dielectric layer to the gate further comprises:

forming an initial opening through the dielectric layer to the conformal etch stop layer;

forming a subsequent opening through the conformal etch stop layer to the gate; and

wherein forming the subsequent opening comprises etching for a period of time between a time necessary to etch through the conformal etch stop layer on the gate region and a time necessary to etch through the conformal etch stop layer and to the junction region.

6. (Original) The method of claim 4, wherein the forming a dielectric layer on the gated device further comprises:

forming a conformal first dielectric layer on the gated device in the active region;

planarizing the first conformal dielectric layer to expose the conformal etch stop layer on a portion of the gate;

forming a different second dielectric layer on the gated device in the active region; and

wherein the forming a contact opening through the dielectric layer and to the gate further comprises:

etching an initial gate contact opening to the different second dielectric layer using an etch chemistry having a greater selectivity for the second dielectric layer than for the first dielectric layer and etch stop layer; and

etching a subsequent gate contact opening through the etch stop layer to the gate.

7. (Original) The method of claim 6, wherein the etching a subsequent gate contact opening comprises etching for a period of time between a time necessary to etch through the etch stop layer on the gate region and a time necessary to etch through the etch stop layer and to the junction region.

8. (Currently Amended) A method for forming a contact opening comprising:

forming an active region;

forming a transistor device within the active region;

forming a dielectric layer on the transistor device in the active region;

forming a contact opening through the dielectric layer to a junction region of the transistor device using a first mask; and

forming a contact opening through the dielectric layer to ~~the~~ a gate of the transistor device in the active region using a different second mask.

9. (Original) The method of claim 8, wherein prior to forming the dielectric layer on the transistor device, forming a conformal etch stop layer on the junction region and the gate of the transistor device.

10. (Currently Amended) The method of claim ~~8~~9, wherein the forming an opening through the dielectric layer further comprises:

forming an initial opening through the dielectric layer to the conformal etch stop layer;

forming a subsequent opening through the conformal etch stop layer to the gate; and

wherein forming the subsequent opening comprises etching for a period of time between a time necessary to etch through the conformal etch stop layer on the gate region and a time necessary to etch through the conformal etch stop layer and to the junction region.